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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,646	10/15/2003	Li-Chun Tu	MTKP0046USA	2645

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NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,646	TU ET AL.	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The instant application having application No. 10/605,646 has a total of 10 claims pending in the application; there are 1 independent claim and 9 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.*

Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,691,219 B2 to Ma et al. (hereinafter Ma).

1. In regard to claim 1, Ma teaches:

"A method for increasing the internal memory in a processor **(e.g., see column 2, lines 11-13 and 54-61)**, the method comprising:"

"(a) providing an extended internal memory in the processor;" **(e.g., see column 2, lines 11- 29; Figs. 3A-3B).** *Ma teaches a method that extends the addressing capability of an 8-bit microcontroller to memory space of up to 16 M bytes capacity.*

"(b) adding bits to stack addresses with a stack pointer generator so that the processor is capable of accessing memory addresses larger than the bit width of the command set of the processor **(e.g., see column 18, lines 1-17; Fig. 5B)**, and can use the extended memory as stack." **(e.g., see column 18, lines 14-17 and 43-50; Fig. 7).** *Ma discloses that by combining (e.g., adding) the stack pointer (SP) value with bits of extended stack pointer (ESP) register the internal memory used for stack can be extended. Fig. 7 shows that by setting the stack address (SA) bit, the stack is being extended to 1K in the internal RAM space (e.g., see element 235 in Fig. 5B).*

2. *In regard to claim 2, Ma teaches:*

"(c) adding bits to data addresses and register addresses with an address extender." **(e.g., see column 18, lines 11-17; Fig. 2A).** *For example Ma teaches that additional data pointers added to support 24-bit memory addressing. A new Address Control (ACON) is added to allow 8051 compatible Microcontroller operates in 16-bit or 24-bit mode of operations.*

3. *In regard to claim 3, Ma teaches:*

"wherein the step (b) further comprising providing a high stack address, and storing the extra bits in the high stack address when the stack address exceeds the limit of the conventional memory." **(e.g., see column 18, lines 11-17; elements 129 and 131 in Fig. 5B).** *For example ESP (element 129 in Fig. 5B) provides a high stack address.*

4. *In regard to claim 4, Ma teaches:*

"wherein the processor is a MCS series processor." **(e.g., see column 3, line 43).** *Intel 8051 Microcontroller taught by Ma is a MCS series processor (e.g., see the paragraph 4 of the Applicant's specification).*

5. *In regard to claim 5, Ma teaches:*

"wherein the CPU processes an 8-bit command set." **(e.g., see column 2, lines 50-51).** *For example all instructions (e.g., commands) are compatible with the 8051-microcontroller instructions set, which is 8-bit instruction set.*

6. *In regard to claim 6, Ma teaches:*

"wherein the conventional memory and the extended memory are in a same block of memory." **(e.g., see column 18, lines 6-8; element 235 in Fig. 5B).**

7. *In regard to claim 7, Ma teaches:*

"wherein the capacity of the conventional memory is 256-bytes." **(e.g., see column 17, lines 45-48).**

8. *In regard to claim 8, Ma teaches:*

"wherein data, registers, and stacks share the conventional memory." **(e.g., see elements 120, 235, and 370 in Fig. 5A).**

9. *In regard to claim 9, Ma teaches:*

"wherein the extended memory is only for storing stacks." **(e.g., see element 235 in Fig. 5B).**

10. *In regard to claim 10, Ma teaches:*

"A chip for executing the method of claim 1." **(e.g., see column 15, lines 34-35).** *The extended addressing method taught by Ma is implemented on Intel 8051, which is a single-chip microcontroller.*

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent No. 5,481,689 to Stamm et al. describes Conversion of internal processor register commands to I/O space addresses.

2. U. S. Patent No. 5,038,280 to Watanabe et al. describes Information processing apparatus having address expansion function.

3. U. S. Patent No. 4,399,507 to Cosgrove et al. describes Instruction address stack in the data memory of an instruction-pipelined processor.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from **8:00 AM to 5:00 PM.**

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information

about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF

NASSER MOAZZAMI
PRIMARY EXAMINER

2005-07-23